TR 921019-2

Technical Report on

"Development of 6H-SiC CMOS Transistors for Insertion into a 350°C Operational Amplifier"

Contract Number:
N00014-92-C-0053

For the Period:
May 16, 1992 - July 15, 1992

Submitted to:

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Source of Funding:

Office of Naval Research

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July 22, 1992

I. Summary

Wafers with epitaxial layers have been grown for both n-channel and p-channel 6H-SiC MOSFETs. The device fabrication for each of these designs is in progress. Both types of devices will utilize ion implanted source and drain wells and will have molybdenum gate contacts that overlap the implanted wells. The same interdigitated mask design will be used for both of the devices. Eight wafers for p-channel devices are being held until the first batch of these devices is completed.

Device parameter measurements have been made on n-channel MOSFET devices that were fabricated prior to this contract. These parameters were to be used to simulate circuits using Simulation Program with Integrated Circuit Emphasis (SPICE). The devices had I-V curves characteristic of normal MOSFETs. However, the gate leakage of these devices was too high to be allow meaningful data to be taken at very low drain biases. Therefore, the wafers currently in process must be finished, and must have sufficiently low gate leakage, before a significant modeling effort can be undertaken.

II. Background

For this Phase I effort, it was proposed to fabricate and characterize both p-channel and n-channel MOSFETs in 6H-SiC. While there has been some development of n-channel MOSFETs in 6H-SiC previous to this effort, they are still in the very early stages of development. To date there have been no p-channel MOSFETs reported in the literature. Therefore, it was proposed to fabricate both types of these devices and then fully characterize them from room temperature to 350°C. This effort would include the development of improved processes for oxide growth and contact annealing for 6H-SiC, as well as the other necessary device fabrication techniques that are required for these devices.

The data obtained for these devices would then be used to model both device parameter optimization and circuit simulation (SPICE) to accurately predict the characteristics that can be expected from a high temperature operational amplifier to be fabricated and tested during Phase II. The device modeling and circuit simulation that was proposed was to be conducted by Dr. John Paulos, an Associate

Professor in the Department of Electrical and Computer Engineering at North Carolina State University (NCSU).

In the previous reporting period, the design of the n- and p-channel devices was discussed. The device pattern utilizes an interdigitated pattern, where the gate contact weaves in between the source and drain fingers, overlapping ion implanted source and drain wells. Four different gate lengths are included on this mask set, being 7 μm, 10 μm, 15 μm, and 20 μm. The gate width for all of these devices is 1 mm.

III. MOSFET Device Development

A. n-channel MOSFETs

Seven wafers have been grown for the fabrication of n-channel MOSFETs. The p-type wafers were sawed from Al-doped p-type 6H-SiC single crystal boules. The substrates were then diamond polished on the (0001) Si-face. The carrier concentration of the substrates ranged from $p = 1.3\text{-}3.3\times10^{18}$ cm^{-3}. Epitaxial thin films of Al-doped 6H-SiC were then grown on the substrates, with a thickness of 3 μm and carrier concentrations in the range of $p = 3\text{-}10\times10^{15}$ cm^{-3}.

After the epitaxial layers were grown, the device fabrication was initiated. The device structure is shown in cross-section in Fig. 1. The source and drain wells were formed by ion implantation of N^+ at high temperature (650°C), using polysilicon as the implant mask. Because of the high temperature anneal required for dopant activation after the ion implantation step, the wafers must be stripped clean. Therefore alignment marks were first reactive ion etched into the wafer surface in order to allow alignment of the patterns to the ion implanted wells after the high temperature anneal. The ion implanted wafers were annealed at 1550°C for 10 minutes. After the anneal, four of the wafers were cleaned and oxidized at 1100°C in wet O_2 for 300 minutes, resulting in an oxide thickness of about 500 Å.

Three of the wafers had about 270 Å of polysilicon deposited on them prior to oxidation, and were then oxidized for a much shorter period of time such that all of the polysilicon was consumed for the formation of the SiO_2, but the oxide growth stopped at the SiC interface. The resulting oxide thickness was about 600 Å. The

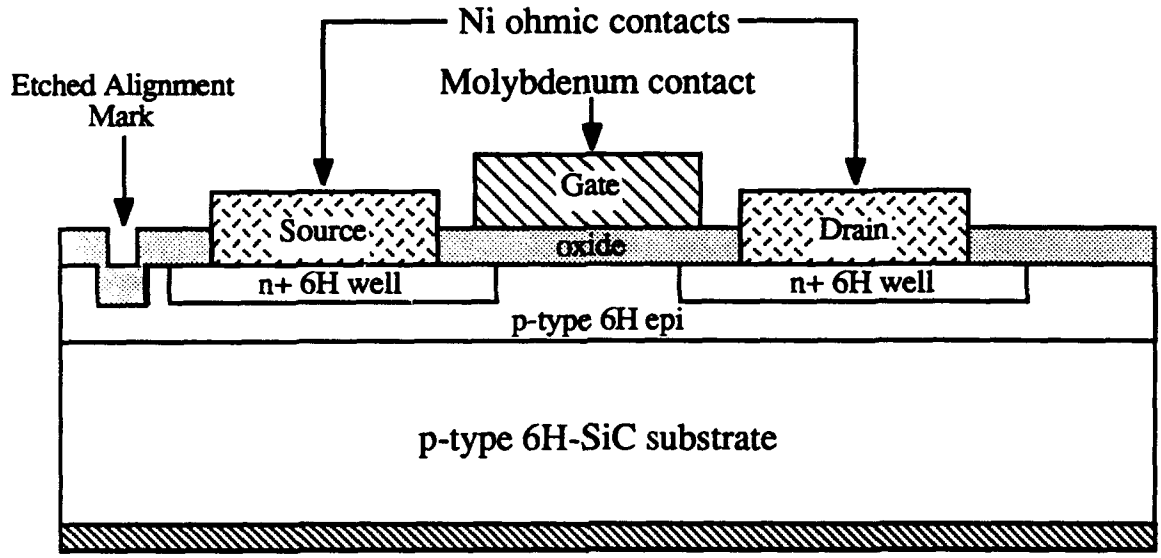

Figure 1: Cross-sectional view of the 6H-SiC n-channel MOSFET design, utilizing ion implanted source and drain wells.

reason for using this "sacrificial" layer of polysilicon for the formation of the gate oxide was to prevent the Al p-type dopant in the SiC from being incorporated into the SiO_2. Recent studies at Cree have shown that Al causes degraded electrical quality in the resulting oxides, particularly in the respect to interface trap density and oxide leakage.

After the oxide layers were grown, the molybdenum gate contacts were deposited and patterned on the wafers, which is the current state of these devices. The final device fabrication procedures will utilize annealed nickel as the source and drain ohmic contact metal. The substrate ground contact on the back of the wafers will be titanium.

B. p-channel MOSFETs

Sixteen wafers have been grown for the fabrication of p-channel MOSFETs. The n-type wafers were sawed from N-doped n-type 6H-SiC single crystal boules. The substrates were then diamond polished on the (0001) Si-face. The carrier

concentration of the substrates ranged from n = 0.5-1.6×10^{18} cm^{-3}. Epitaxial thin films of N-doped 6H-SiC were then grown on the substrates, with a thickness of 3 μm and carrier concentrations in the range of n = 3-40×10^{15} cm^{-3}. This wide variation in channel doping was used to allow insight into the effect of the channel doping on the I-V characteristics.

As was the case for the n-channel MOSFETs, the device fabrication for eight of the p-channel MOSFETs has been initiated. The other eight wafers will be held until the first batch is completed. The second batch will be processed with any necessary improvements that are discovered during the fabrication of the first batch, if enough time and money are left in the Phase I effort. If not, these wafers will be saved for the Phase II effort that will be proposed. The device structure for these wafers is shown in cross-section in Fig. 2. The source and drain wells were formed by ion implantation of Al^+ at high temperature (650°C), again using polysilicon as the implant mask. These implants were then given a high temperature anneal for dopant activation after the ion implantation step.

All of the wafers were then coated with a thin layer of polysilicon to be used for oxide consumption, as was discussed for the n-channel wafers. The reason this is necessary for the p-channel devices is not due to the n-type channel material, but rather to the fact that the gate must overlap the p^+ source and drain. These areas are doped very heavily with Al and when they are oxidized the resulting SiO_2 has very poor insulating quality. When previous attempts at p-channel devices were made at Cree using conventional oxidation, the gates had very high leakage currents because of the poor oxide quality on the p^+ well overlap. Therefore, the SiO_2 layers were grown from the polysilicon layers and the oxide growth was stopped at the SiC interface. Like the n-channel devices the resulting SiO_2 thickness was about 600 Å.

After the oxide layers were grown, the molybdenum gate contacts were deposited and patterned on the wafers, which is the current state of these devices. The final device fabrication procedures will utilize a proprietary aluminum-based alloy as the source and drain ohmic contact metal. The substrate ground contact on the back of the wafers will be nickel.

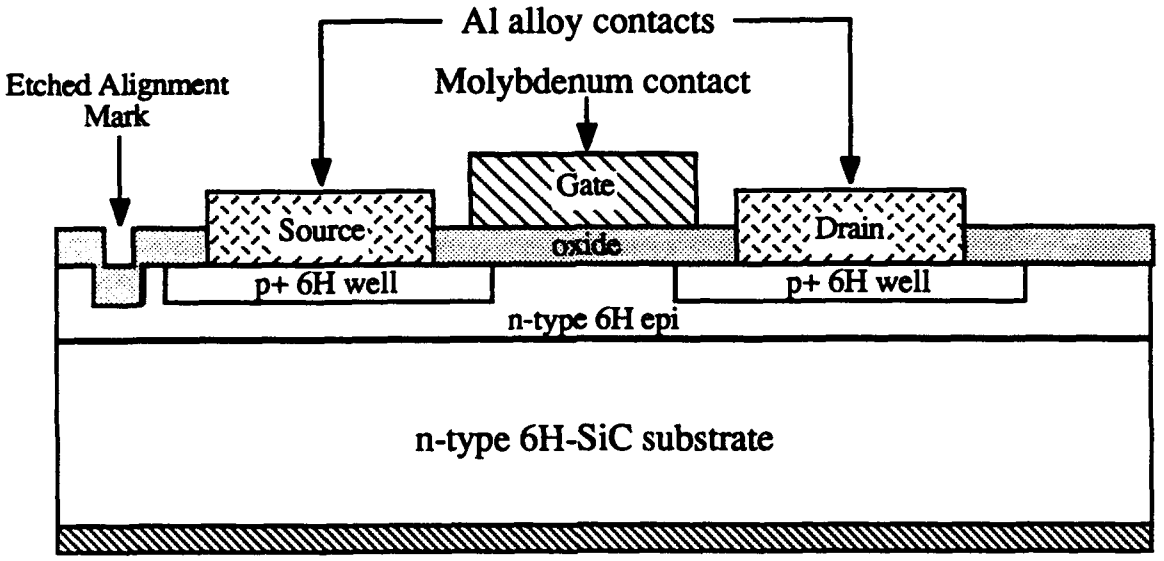

Figure 2: Cross-sectional view of the 6H-SiC p-channel MOSFET design, utilizing ion implanted source and drain wells.

IV. Initial Modeling for 6H-SiC CMOS Operational Amplifier

A feasibility study has been performed in conjunction with Dr. John J. Paulos and his graduate student Tricia Eckman, both of North Carolina State University, to investigate possible ways to design circuits using both NMOS and PMOS transistors (complementary process) in silicon carbide. Three approaches were discussed in the previous report. The first was a hybrid approach in which NMOS and PMOS transistors are fabricated on separate wafers. These wafers would be sliced into individual die and packaged together using bond wires to interconnect the NMOS and PMOS devices.

A second approach would utilize a shared substrate in which both NMOS and PMOS transistors are fabricated on a p-type wafer with an n-type epitaxial layer. With this approach, the PMOS transistor is a true enhancement-mode MOSFET and the NMOS transistor (fabricated in n-type material) acts as a depletion-mode device and can be modeled as a MOSFET in parallel with a body resistor. This approach appears to be the least favorable due to the added complexity of selective etching and the poor performance of the NMOS transistor.

The last approach studied was a true complementary process using multiple epitaxial layers to provide each transistor with the appropriate substrate material. A p-type epitaxial layer would be grown on a p-type substrate for fabrication of the NMOS transistor. An n-type epitaxial layer would then be grown on the p-type epitaxial layer for fabrication of the PMOS transistors. The n-type layer would be etched to form mesas for the PMOS transistor. An extra contact for each layer has to be provided in order to properly bias each "substrate". This approach is the most promising from a circuit performance standpoint as both the NMOS and the PMOS devices are true enhancement-mode MOSFETs.

In order to properly simulate circuits using SPICE (Simulation Program with Integrated Circuit Emphasis), models must be developed that reflect the characteristics of the devices to be used. Individual NMOS transistors which had been fabricated previous to this contract were tested at room temperature and at elevated temperature (up to 350°C) to determine their operating characteristics. Typical I-V curves for the n-channel devices were presented in the previous report.

While these devices have all the characteristics of a typical MOSFET curve, one important problem area for these devices is the unusually high gate leakage currents. The gate leakage current is often in the range of 500 μA when the gate bias is increased to +15 V. Thus, when the drain is fixed at very low bias voltages, the gate leakage is the dominating influence on the device and the I-V curves do not behave as those of a typical Si MOSFET. Unfortunately, it is this low drain bias condition that is favored for the measurements required for the modeling efforts. Therefore, the parts that were provided to NCSU, and were measured using TECAP (Transistor Electrical Characterization and Analysis Program), were determined to have gate leakage too high to allow meaningful measurements to be taken.

Further modeling efforts will require that the new batch of MOSFETs, discussed in Section III, be finished and characterized. Hopefully, these new devices will not have the high gate leakage levels and will allow the low drain bias measurements to be taken without the influence of gate leakage.

V. Plans for Next Period

Fabrication of the n-channel and p-channel MOSFETs discussed in Section III will be continued and finished during the next month. These devices will then be fully characterized so the device parameters can be included in the SPICE modeling effort. Parameter optimization will be performed to obtain SPICE level 3 parameters which provide good fit to the experimental data. Of particular interest will be the characterization of the p-channel devices, since none have been successfully fabricated to date and their is no reported characteristics for these devices.

SPICE will be used to design an operational amplifier (opamp) using the models developed for the silicon carbide transistors. Two of the three process approaches discussed earlier will be used to show two possible opamp designs. A hybrid opamp will be designed using the silicon carbide device models and incorporating parasitic capacitances associated with hybrid packaging, and a true complementary opamp will be designed using the same silicon carbide device models and incorporating small on-chip parasitic capacitances.

Circuit performance will be assessed to determine the impact of the hybrid parasitics and to identify possible changes in processing to improve device performance. Feedback will be provided from the transistor testing and circuit design to the proposed Phase II experimental effort.